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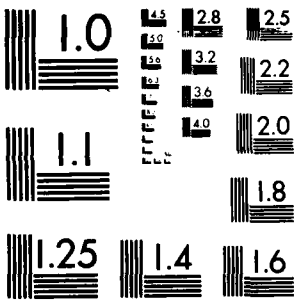

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Aero Propulsion Technical Memorandum 423

A PHASE-LOCKED FREQUENCY MULTIPLIER FOR THE SIGNAL AVERAGING OF THE VIBRATION OF THE WESSEX HELICOPTER INPUT SPIRAL BEVEL PINION

by

P. D. McFADDEN

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A PHASE LOCKED FREQUENCY MULTIPLIER FOR THE SIGNAL AVERAGING OF THE VIBRATION OF THE WESSEX HELICOPTER INPUT SPIRAL BEVEL PINION

P. D. McFADDEN

SUMMARY

Details are given of the design of a phase-locked frequency multiplier for the conversion of a signal derived from the alternator of the Wessex helicopter into a pulse train suitable for controlling the sampling and signal averaging by a computer of the vibration of the input spiral bevel pinion in the Wessex main rotor gearbox. The frequency multiplier is implemented as a series of four phase-locked loops, and features an oscillator which maintains the loops at approximately the correct frequency in standby mode thereby reducing the time to lock when the input signal is applied.

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1. INTRODUCTION

The calculation of the signal average of the vibration of a gear requires a pulse train which is locked in phase with the rotation of the gear of interest and has an integer number of pulses per revolution of that gear. While it is sometimes possible to obtain a signal giving one or more pulses per revolution directly from the gear of interest or from its shaft, it is not infrequently found that these components are inaccessible. It is then necessary to obtain a signal from some other shaft or gear in the system and to convert it to the required signal by a phase-locked frequency multiplier.

The input spiral bevel pinion gear in the main rotor gearbox of the Wessex helicopter is an example. The input shaft to the gearbox to which the pinion is coupled is not readily accessible, but there are other signals available from the gearbox, including the output of the alternator which may be obtained from outlets in the aircraft cabin. As the main rotor of the aircraft operates at a nominally constant speed, the alternator has no speed governor, and so produces an output frequency which is directly proportional to the rotation frequency of the input bevel pinion. In principle, it is possible to convert the measured speed signal to the desired signal by a single stage of multiplication and a single division, with the ratios being determined uniquely by the numbers of teeth on the gears linking the source of the speed signal with the gear of interest. There are commercial instruments available, such as the Spectral Dynamics SD134A Tracking Ratio Tuner, which provide a single multiplication and division. The SD134A permits multiplication by integers from 1 to 2000 and division by numbers from 1 to 9999, and selecting the desired ratio automatically sets the response characteristic of the instrument.

Trials with the SD134A on recorded Wessex data have revealed some serious problems. Firstly, the limited range of multiplication greatly restricts the number of samples per revolution of the input bevel pinion which can be achieved. As subsequent processing of the signal averages makes extensive use of the fast Fourier transform, a considerable saving in analysis time can be achieved by selecting a number of points per revolution which is a power of two. Using the SD134A and the alternator signal, this cannot be achieved. Secondly, the response of the instrument to small speed variations appears to be underdamped. Consequently, any noise on the recording of the alternator signal is sufficient to cause the multiplier to lose phase lock and corrupt the signal average. Hence there is a clear need for a phase-locked frequency multiplier designed expressly for the conversion of the alternator signal into a form suitable for the signal averaging of the vibration of the Wessex input bevel pinion, with a response characteristic designed to perform satisfactorily in the presence of small amounts of noise. This technical memorandum describes the design and construction of such a multiplier.

2. REQUIREMENTS

The following subsections describe the requirements of each of the stages of the phase-locked frequency multiplier.

2.1 Input Signal

The frequency of the alternator output of the Wessex main rotor gearbox at 100% rated speed is 400 Hz. The signal from each phase is approximately sinusoidal, although there are higher harmonics present at low levels. As part of the RAN Recorded Tape Vibration Analysis Program, the attenuated alternator signal is recorded using frequency modulation on channel 4 of a Bruel and Kjaer 7003 tape recorder at 15 inches per second (ips). On playback the amplitude of the signal is less than 1 V.

In practice it has been found that 400 revolutions of the input bevel pinion are sufficient to provide a stable signal average. Given that the nominal rotation frequency of the pinion is 42.7 Hz, the time required for data capture is less than 10 s in real time. For the present implementation of the signal averaging technique, it has been decided to replay the tape at 1.5 ips to allow the operator to monitor the process more effectively. The data capture time is therefore approximately 100 s and the nominal frequency of the input to the multiplier is 40 Hz. Hence the input stage of the multiplier must be designed to accept a noisy sinusoidal signal at 40 Hz.

2.2 Multiplication

The input bevel pinion gear in the Wessex main rotor gearbox has 22 teeth. Studies of vibration spectra made from RAN recordings indicate that the fundamental and second harmonic of the tooth meshing frequency predominate, but that higher harmonics can also be present at low levels. To permit efficient processing of the signal average by the fast Fourier transform, it is desirable that the number of samples per revolution be a power of two, such as 64, 128, 256, 512,... The smallest number of samples per revolution meeting this criterion which can adequately resolve the fourth harmonic of the tooth meshing frequency is 256. Hence the phase-locked frequency multiplier should produce at least 256 pulses per revolution of the input bevel pinion.

Figure 1 shows a schematic view of some of the major gears in the main rotor and accessory gearboxes of the Wessex helicopter, including the numbers of teeth on the gears. The alternator has three poles, therefore the rotation frequency I of the input bevel pinion can be related to the alternator output frequency A by the following equation:

$$I = (A/3) \times (57/22) \times (21/61) \times (44/122) \qquad (1)$$

The sampling frequency S=256I is given by:

$$S = (A/3) \times (57/22) \times (21/61) \times (44/122) \times 256 \qquad (2)$$

After eliminating common factors and rearranging, this becomes:

$$S = A \times ((\ 3 \times 7 \times 19\ )/(\ 61 \times 61\ ))\ \times 256 \qquad (3)$$

Tests using the recorded alternator signal and a breadboard model of the multiplier circuit showed that multiplication by more than approximately 21 in any single stage produced unacceptable phase jitter at the output of that stage which often prevented the following stage from locking. Arranging the factors in the numerator to meet this criterion required four multiplier stages of 19,21,16 and 16. It was also found that by placing the factors 61 and 61 in the denominator in the first two stages, the jitter inherent in the recorded signal could be more effectively suppressed, albeit at the expense of a greater lock time. The factors were therefore arranged as follows:

$$S = A \times (19/61)_1 \times (21/61)_2 \times (16)_3 \times (16)_4 \qquad (4)$$

2.3 Output Signal

The sampling and signal averaging of the gearbox vibration is performed by a Digital Equipment Corporation (DEC) LSI11 computer system. The analogue-to-digital converter in the system requires a TTL-compatible signal to control the sampling and conversion of the vibration signal. In order to reduce the risk of interference from other sources causing spurious samples to be taken, the output impedance of the phase-locked frequency multiplier should be low. The output should also be able to withstand accidental short-circuits without damage.

3. DESCRIPTION

The following subsections describe the operation of each of the stages of the phase-locked frequency multiplier.

3.1 General

Figure 2 shows a block diagram of the phase-locked frequency multiplier designed to meet the requirements of the previous section. The input stage comprises an inverting amplifier and a Schmitt trigger to convert the analogue alternator signal to a digital square wave signal compatible with the subsequent CMOS devices. After the input stage there follow four separate CMOS phase-locked loops which implement equation 4.

The output stage converts the CMOS-level signals to a TTL-compatible signal with low output impedance. The lock indicator senses and displays the occurrence of an out-of-lock condition in any of the phase-locked loops. The standby oscillator produces a CMOS-compatible square wave signal at the nominal alternator frequency so that the phase-locked loop stages can be maintained at approximately the correct frequency thereby reducing the time required for the loops to lock when the input signal is applied.

3.2 Input Stage

The circuit diagram of the input stage is shown in Figure 3. The input signal is AC coupled by a 0.47 µF capacitor to an amplifier with a gain of 10, thereby ensuring that the level of the signal is sufficient for the next stage. The amplifier consists of an LM3900 Norton amplifier operating from the single +5 V supply rail and connected as an inverting amplifier. The quiescent output voltage is biased to about +2.5 V by the 2.7 MΩ resistor to +5 V in the positive input of the amplifier. The output of the amplifier is connected via a 0.47 µF coupling capacitor to a CMOS 74C914 Schmitt trigger. On a +5 V supply the Schmitt trigger has switching levels of +1.3 V and +3.7 V, and it is this hysteresis which reduces the effect of noise in the incoming signal on the frequency multiplier stages.

3.3 Multiplier Stage

The circuit diagram of the multiplier stage is shown in Figure 4. Each of the four multiplier stages is of the same design but with differing divider preloads and voltage-controlled oscillator (VCO) and loop filter components. The first part of the multiplier consists of a CD4046B phase-locked loop and a programmable divider. The CD4046 features two different phase detector configurations. The one used in this design, designated type II, is an edge-triggered digital network

which responds to the leading edges of the incoming pulses. The maximum frequency of the VCO for a given supply voltage is determined solely by a single external resistor and capacitor. These components have been selected to give a maximum VCO frequency which is approximately double the normal operating frequency, as described in a later section. The output signal from the phase detector is connected to the input of the VCO via a second-order filter, the cutoff frequency and damping of which determine the response of the multiplier. The selection of the filter components is described in a later section.

The output of the VCO is connected to the input of a programmable divider which consists of two CD4029 presettable, binary/decade up/down counters configured as a binary down ripple counter. The carry output of the most significant digit is inverted by a 74C04 inverter and applied to the preset inputs of both CD4029 devices. When the counter reaches zero the carry output goes low causing the value M set up by wire-wrapped jumpers to be loaded into the counter. The output of the divider is connected to one input of the phase detector where it is compared with the input signal which comes from the previous stage, so that when the loop stabilizes the VCO output frequency will be M times the input frequency. The output of the VCO may also be connected to a second divider network having the same configuration as the first but with a load value D. The output of this second divider has a frequency which is M/D times that of the input to the phase detector. Where D=1 the second divider may be bypassed by a wire-wrapped jumper.

When a phase error occurs between the two input signals to the phase detector, the phase pulse output of the CD4046 goes low. As this is usually a very short pulse it can be difficult to display effectively, but by connecting the phase pulse output to the D input of a CD4013 dual D latch and the VCO output to the clock input of the latch, the phase pulse can be stretched. If a phase error exists at the leading edge of a VCO output pulse, the error will be latched and held until the next leading edge of the VCO input. The latch output is used to illuminate an on-board LED when a phase error occurs. The latch output is also passed to the main lock indicator circuit.

3.4 Output Stage

The circuit diagram of the output stage is shown in Figure 5. The CMOS output of the multiplier stage is not suitable for driving a TTL load and the high output impedance makes the output sensitive to interference from other sources. By connecting the output of the last multiplier to a 74LS04 inverter and then to a 7407 open-collector TTL buffer with 220 Ω pull-up and 330 Ω pull-down resistors, a low impedance output with good short-circuit immunity is produced.

3.5 Lock Indicator

Figure 6 shows the circuit diagram for the lock indicator. It consists of a CMOS 8-input 74C30 NAND gate which accepts the lock signals from the four multiplier stages. The remaining inputs are wired

high but could be used for additional multiplier stages. The output of the NAND gate operates a high-efficiency LED mounted on the front panel. When any one or more of the multiplier stages loses phase-lock the LED illuminates.

3.6 Standby Oscillator

Figure 7 shows the circuit diagram for the standby oscillator, which consists of an NE556 precision timer connected as a free-running oscillator with approximately 50% duty cycle. The output frequency is tuned to 40 Hz by a trimpot. The input of the first multiplier stage is connected via an SPDT toggle switch on the front panel to either the conditioned input signal or to the standby oscillator. When no input signal is applied, setting the switch to the standby position causes the multiplier stages to stabilize close to the normal operating range. After the input signal is applied, the switch is changed to the operate position, and because the multipliers are already close to the correct frequency, lock will be achieved quickly, typically within 20 s. Without the standby oscillator, the VCO output frequencies would decrease slowly until they reached their minimum operating frequencies. When the input signal was applied, the time to achieve lock would be excessive.

If required, remaining sections of the LM3900 and NE556 could be configured as a level detector or missing pulse detector to automatically switch between standby and operate modes.

3.7 Power Supply

For simplicity, a single +5 V power supply is used, provided by a plug pack giving 9 V AC at 200 mA, a full-wave rectifier and LM317T voltage regulator. The power supply circuit is shown in Figure 8.

4. MULTIPLIER DESIGN

This section describes the component selection procedures for the VCO and loop filter of each multiplier stage.

4.1 VCO Component Selection

Consider the first multiplier stage, which multiplies by 19 and divides by 61. The nominal input frequency f_i is 40 Hz, hence the normal VCO output frequency will be f_c=40x19=760 Hz. A suitable maximum VCO frequency f_o is 2 kHz. From performance charts for the CD4046 [1], it can be seen that for a +5 V supply:

$$f_o \simeq 1/(R_0 C_0) \tag{5}$$

where R_0 and C_0 are the VCO resistor and capacitor. If C_0=1 nF, this equation yields R_0=500 kΩ. Using the above procedure, the VCO components shown in Table 1 can be selected.

4.2 Filter Component Selection

The natural frequency w_n and damping ratio r_d of a phase-locked loop are given by [2,3]:

$$w_n \simeq \sqrt{(K_0 K_0)/T_1} \tag{6}$$

$$r_d = 0.5\, w_n T_2 \tag{7}$$

where $T_1 = R_1 C_1$
$T_2 = R_2 C_1$
$K_0 K_0$ = DC loop gain

The components R_1, R_2 and C_1 are indicated in Figure 4. The loop gain $K_0 K_0$ is approximately given by:

$$K_0 K_0 = f_o / M \tag{8}$$

where M = loop multiplication

Consider the first multiplier stage for which f_o=2 kHz and M=19. Choosing R_1=1 MΩ and C_1=22 μF gives T_1=22 s. Since f_o=2 kHz, substitution in equation 6 yields w_n=2.19 rad/s and f_n=0.35 Hz. Because the ratio f_i/f_o=40/0.35>100, there should be good rejection of jitter on the input signal. Substituting in equation 7 gives r_d=2.19T_2/2. If r_d>1, then T_2>2/2.19 and R_2>41 kΩ. Using the above procedure, the filter components shown in Table 2 can be selected.

5. ACKNOWLEDGEMENTS

The author wishes to thank G.F.Forsyth for his advice and comments and K.W.Vaughan for designing the power supply and building the prototype.

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2. Mills,T.B., 'The Phase Locked Loop IC as a Communication System Building Block', National Semiconductor, Application Note AN-46, June 1971.

3. Nash,G., 'Phase-Locked Loop Design Fundamentals', Motorola Semiconductor Products, Application Note AN-535, 1970.

Table 1 VCO Frequencies and Components

Stage	f_1 Hz	f_c Hz	f_a Hz	Ratio	f_o Hz	R_0 Ω	C_0 nF
1	40	760	2k	19/61	12.5	500k	1
2	12.5	262	1k	21/61	4.3	1M	1
3	4.3	68.8	200	16	68.8	5M	1
4	68.8	1100	2k	16	1100	500k	1

Table 2 Filter Frequencies and Components

Stage	f_a Hz	R_1 Ω	C_1 µF	w_n rad/s	f_n Hz	f_1/f_n	R_2 Ω
1	2k	1M	22	2.19	0.35	114	41k
2	1k	4.7M	22	0.679	0.108	115	134k
3	200	6.8M	22	0.289	0.046	93	314k
4	2k	1M	22	2.38	0.379	211	38k

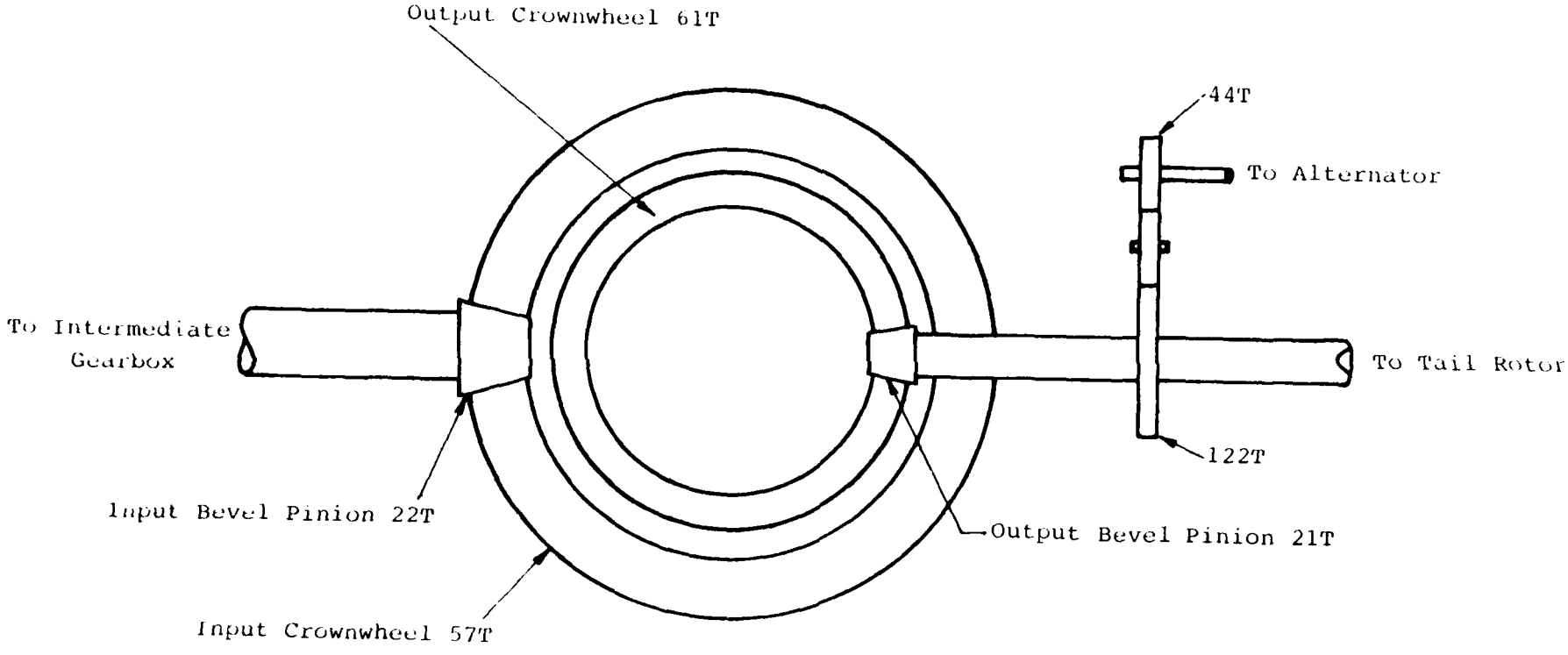


FIG. 1 SOME MAJOR GEARS IN WESSEX MAIN ROTOR AND ACCESSORY GEARBOXES

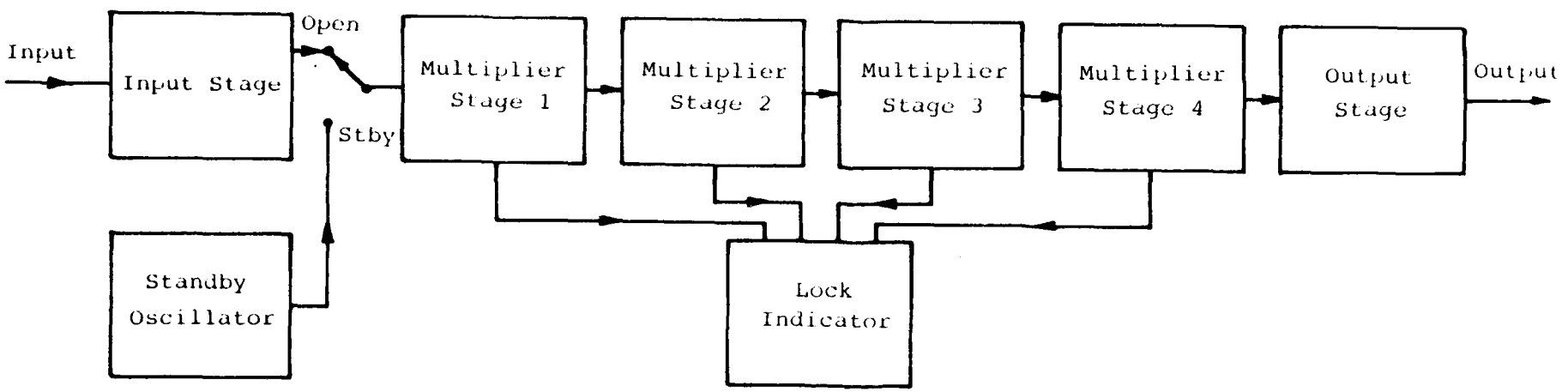


FIG. 2 BLOCK DIAGRAM OF PHASE-LOCKED FREQUENCY MULTIPLIER

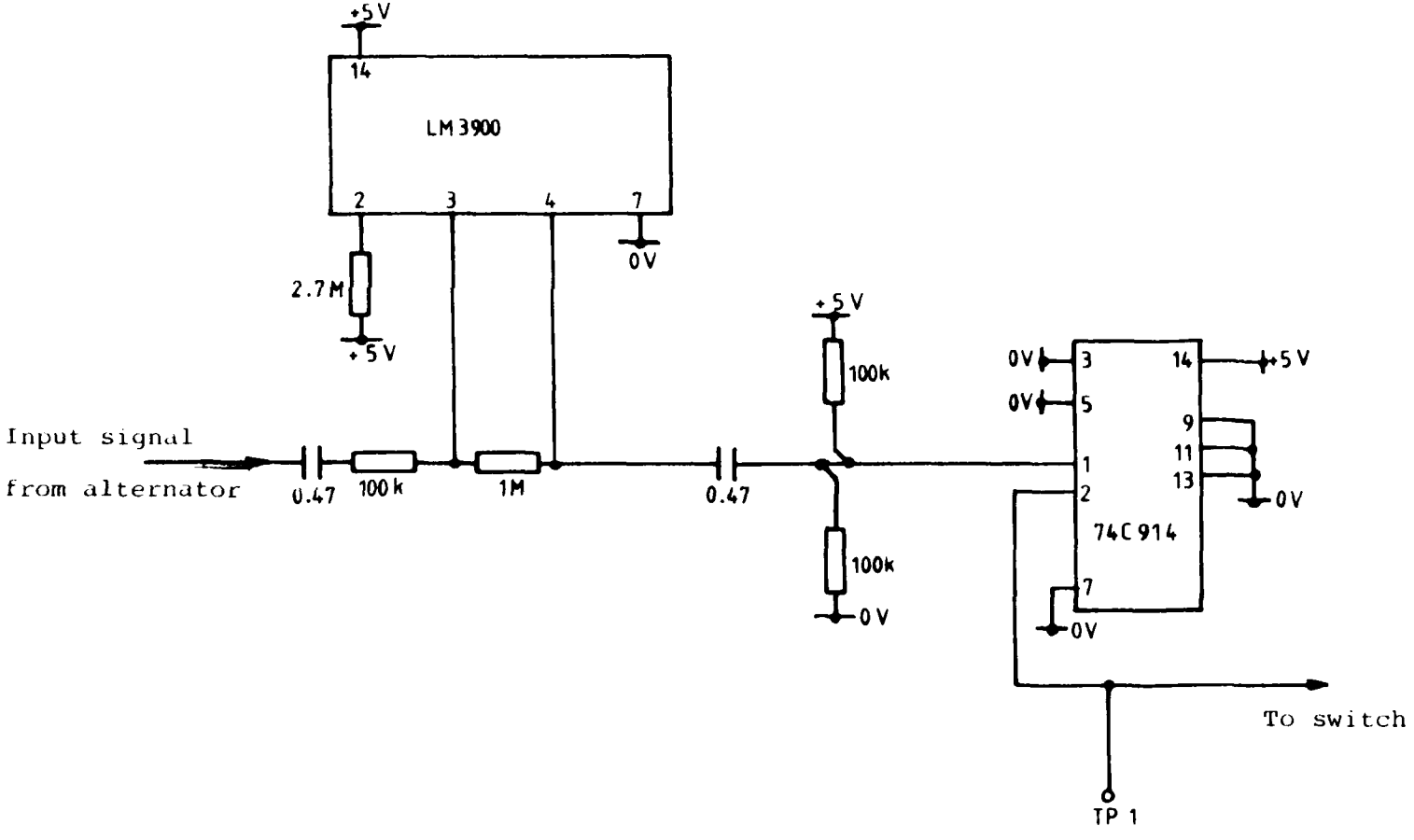


FIG. 3 INPUT STAGE

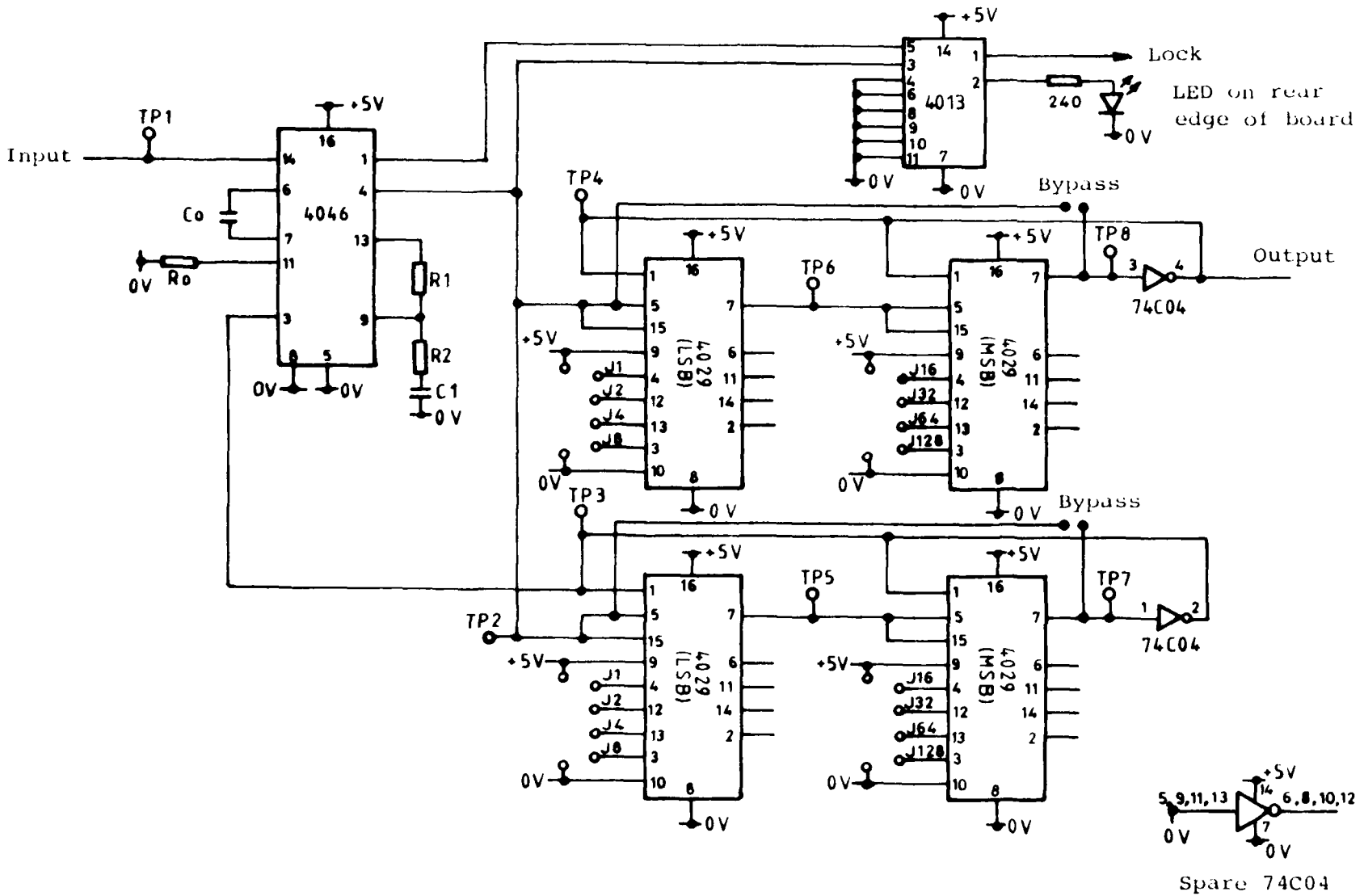


FIG. 4 MULTIPLIER STAGE

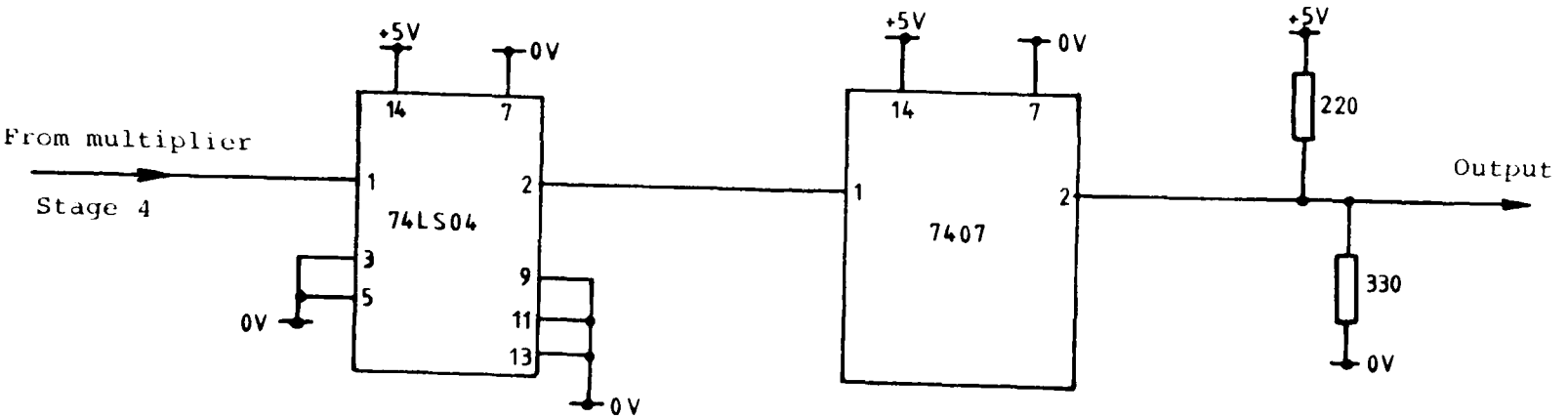


FIG. 5 OUTPUT STAGE

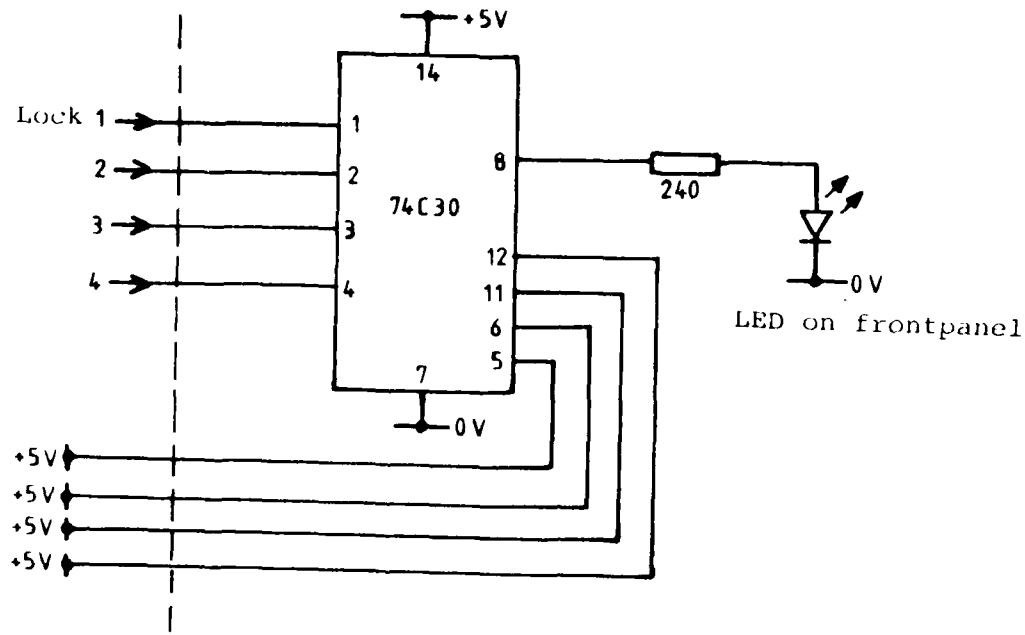


FIG. [illegible] LOCK INDICATOR

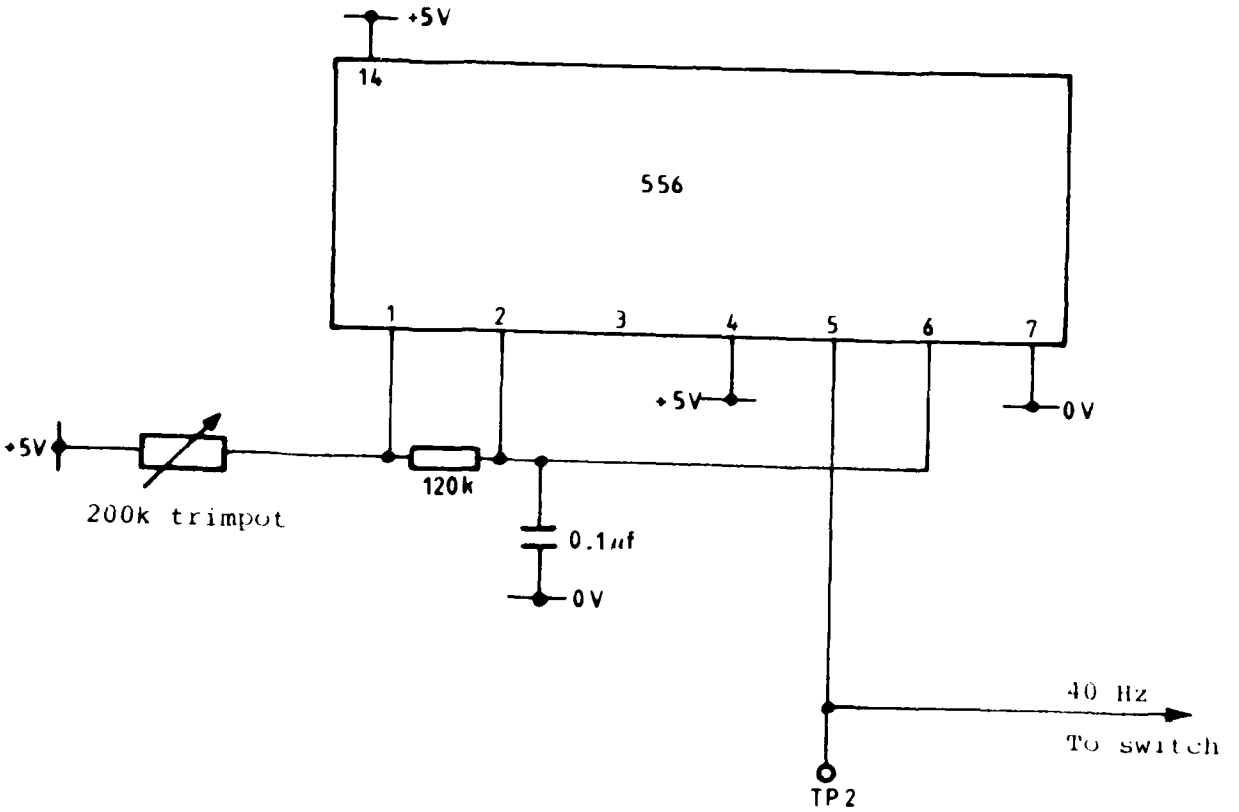
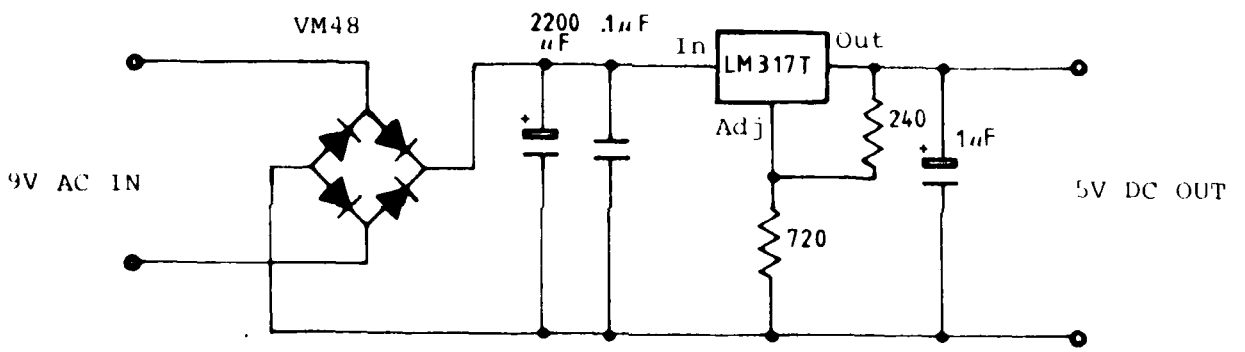


FIG. 7 STANDBY OSCILLATOR



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16. Abstract

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